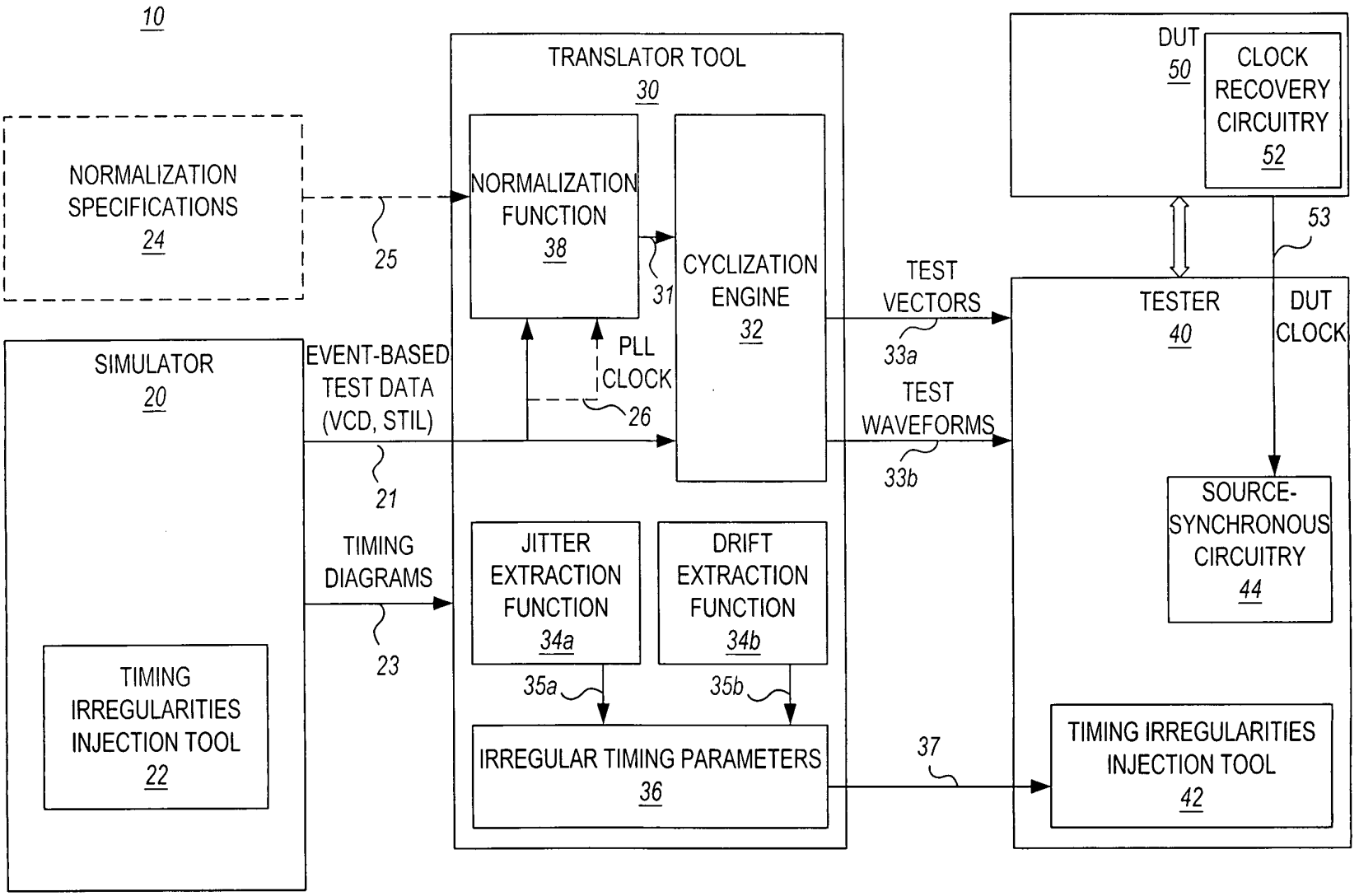
10
NORMALIZATION SPECIFICATIONS 24
25
TRANSLATOR TOOL 30
NORMALIZATION FUNCTION 38
31
CYCLIZATION ENGINE 32
DUT 50
CLOCK RECOVERY CIRCUITRY 52
53
TEST VECTORS
33a
TESTER 40
DUT CLOCK
SIMULATOR 20
EVENT-BASED TEST DATA (VCD, STIL)
PLL CLOCK
26
TEST WAVEFORMS
33b
21
SOURCE-SYNCHRONOUS CIRCUITRY 44
TIMING DIAGRAMS
JITTER EXTRACTION FUNCTION 34a
DRIFT EXTRACTION FUNCTION 34b
23
35a
35b
TIMING IRREGULARITIES INJECTION TOOL 22
IRREGULAR TIMING PARAMETERS 36
37
TIMING IRREGULARITIES INJECTION TOOL 42

FIG. 1

```
$ date
        2/28/2004 1:30:15 PM
$end

$version
        Example Clean Receive Data
$end

$timescale
        1ps
$end

$scope module U $end
$var wire 1 !!RxD ReceiveData $end
$upscope $end

$enddefinitions $end

#0
$dumpvars
1!!RxD
$end
#70
0!!RxD
#120
1!!RxD
#170
0!!RxD
#220
1!!RxD
#270
0!!RxD
```

FIG. 2A

```
$ date
        2/28/2004 1:30:15 PM
$end

$version
        Example Clean Receive
Data
$end

$timescale
        1ps
$end

$scope module U $end
$var wire 1 !!RxD ReceiveData
$end
$upscope $end

$enddefinitions $end

#0
$dumpvars
1!!RxD
$end
#75
0!!RxD
#125
1!!RxD
#165
0!!RxD
#230
1!!RxD
#265
0!!RxD
```

FIG. 3A

```
$ date
        2/28/2004 1:30:15 PM
$end

$version
        Example Clean Receive Data
$end

$timescale
        1ps
$end

$scope module U $end
$var wire 1 !!RxD ReceiveData $end
$upscope $end

$enddefinitions $end

#0
$dumpvars
1!!RxD
$end
#75
0!!RxD
#130
1!!RxD
#185
0!!RxD
#240
1!!RxD
#295
0!!RxD
```

FIG. 4A

```
$ date
        2/28/2004 1:30:15 PM
$end

$version
        Example Clean Receive Data
$end

$timescale
        1ps
$end

$scope module U $end
$var wire 1 !!RxD ReceiveData $end
$upscope $end

$enddefinitions $end

#0
$dumpvars
1!!RxD
$end
#80
0!!RxD
#135
1!!RxD
#180
0!!RxD
#250
1!!RxD
#290
0!!RxD
```

FIG. 5A

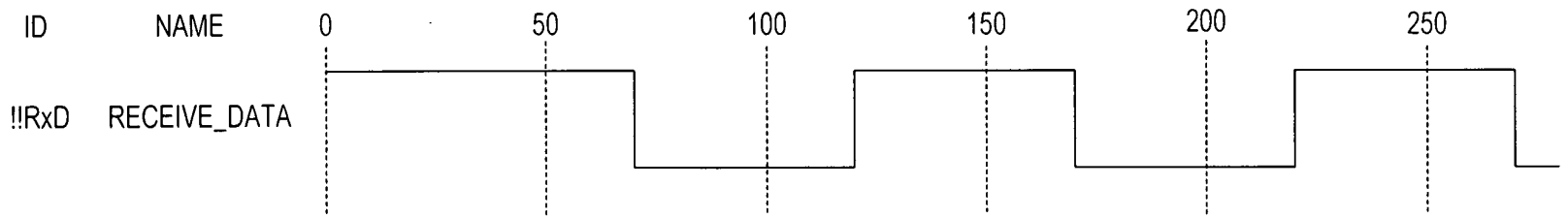

FIG. 2B

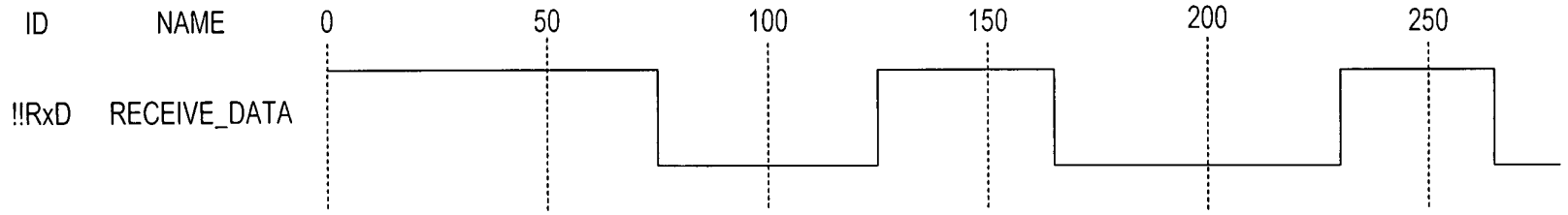

FIG. 3B

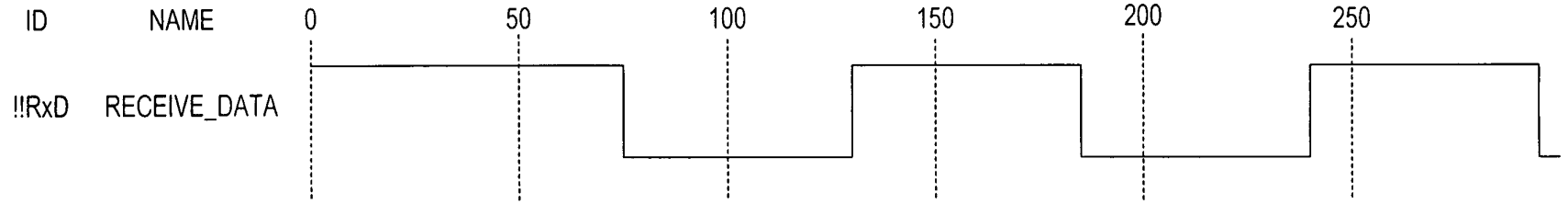

FIG. 4B

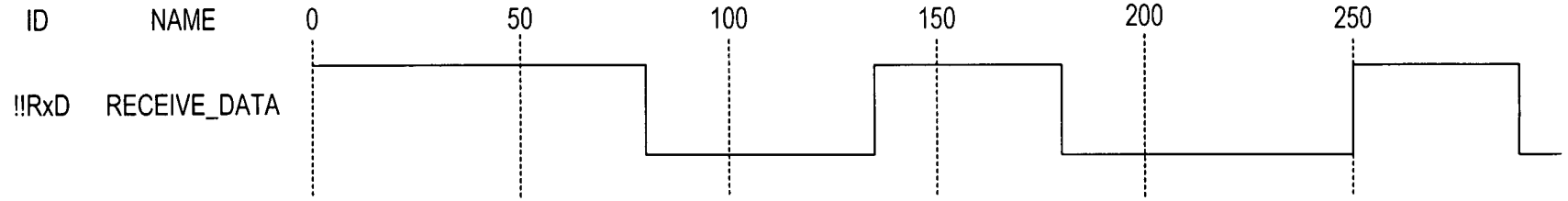

FIG. 5B

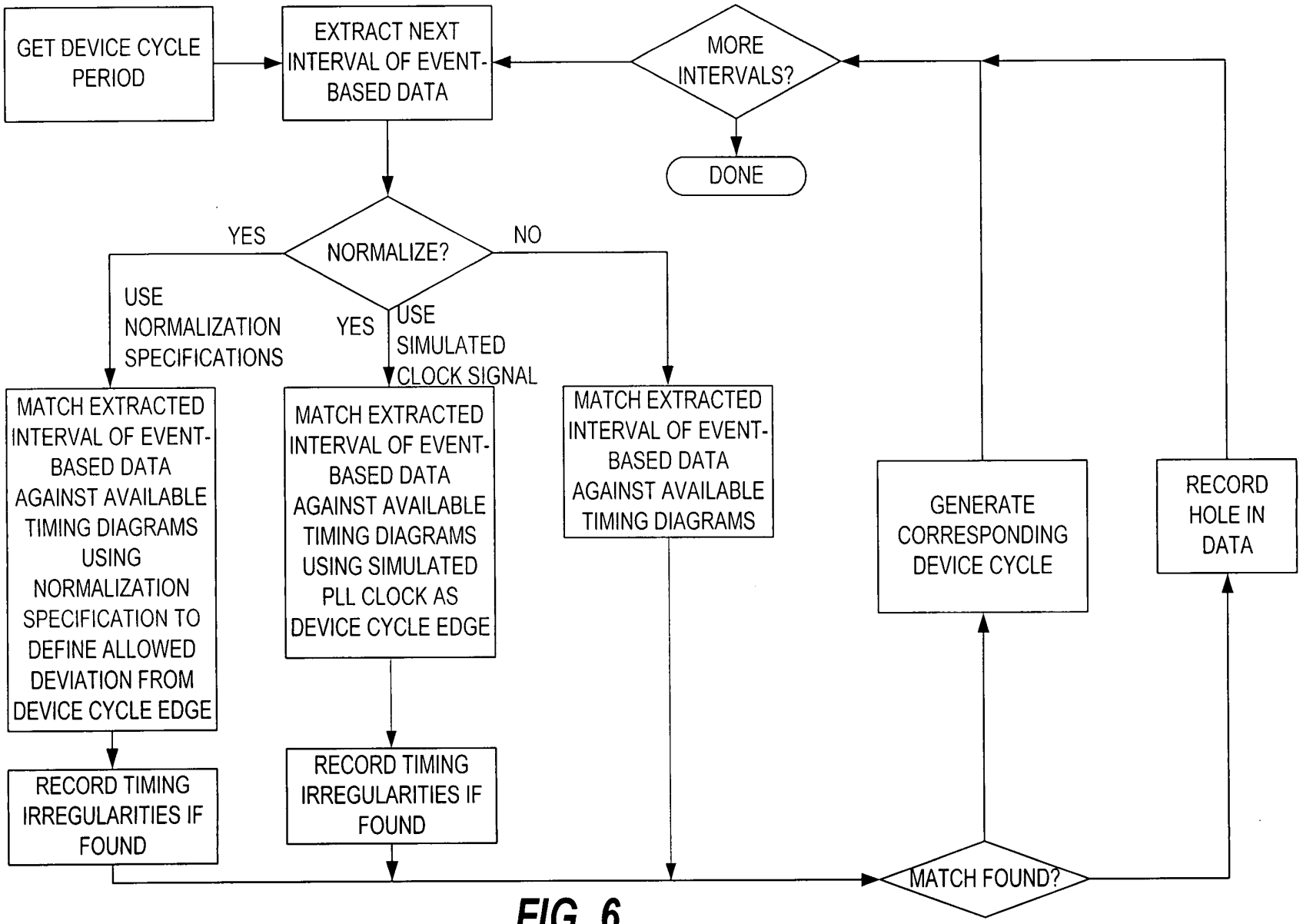
GET DEVICE CYCLE PERIOD
EXTRACT NEXT INTERVAL OF EVENT-BASED DATA
MORE INTERVALS?
DONE
NORMALIZE?
YES
NO
USE NORMALIZATION SPECIFICATIONS
YES
USE SIMULATED CLOCK SIGNAL
MATCH EXTRACTED INTERVAL OF EVENT-BASED DATA AGAINST AVAILABLE TIMING DIAGRAMS USING NORMALIZATION SPECIFICATION TO DEFINE ALLOWED DEVIATION FROM DEVICE CYCLE EDGE
MATCH EXTRACTED INTERVAL OF EVENT-BASED DATA AGAINST AVAILABLE TIMING DIAGRAMS USING SIMULATED PLL CLOCK AS DEVICE CYCLE EDGE
MATCH EXTRACTED INTERVAL OF EVENT-BASED DATA AGAINST AVAILABLE TIMING DIAGRAMS
RECORD TIMING IRREGULARITIES IF FOUND
RECORD TIMING IRREGULARITIES IF FOUND
GENERATE CORRESPONDING DEVICE CYCLE
RECORD HOLE IN DATA
MATCH FOUND?

FIG. 6

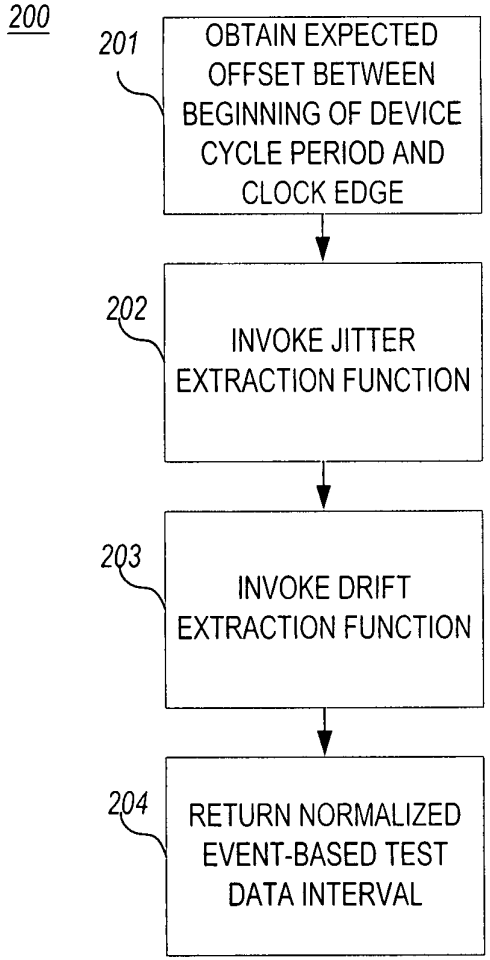
200
201
OBTAIN EXPECTED OFFSET BETWEEN BEGINNING OF DEVICE CYCLE PERIOD AND CLOCK EDGE
202
INVOKE JITTER EXTRACTION FUNCTION
203
INVOKE DRIFT EXTRACTION FUNCTION
204
RETURN NORMALIZED EVENT-BASED TEST DATA INTERVAL

FIG. 7

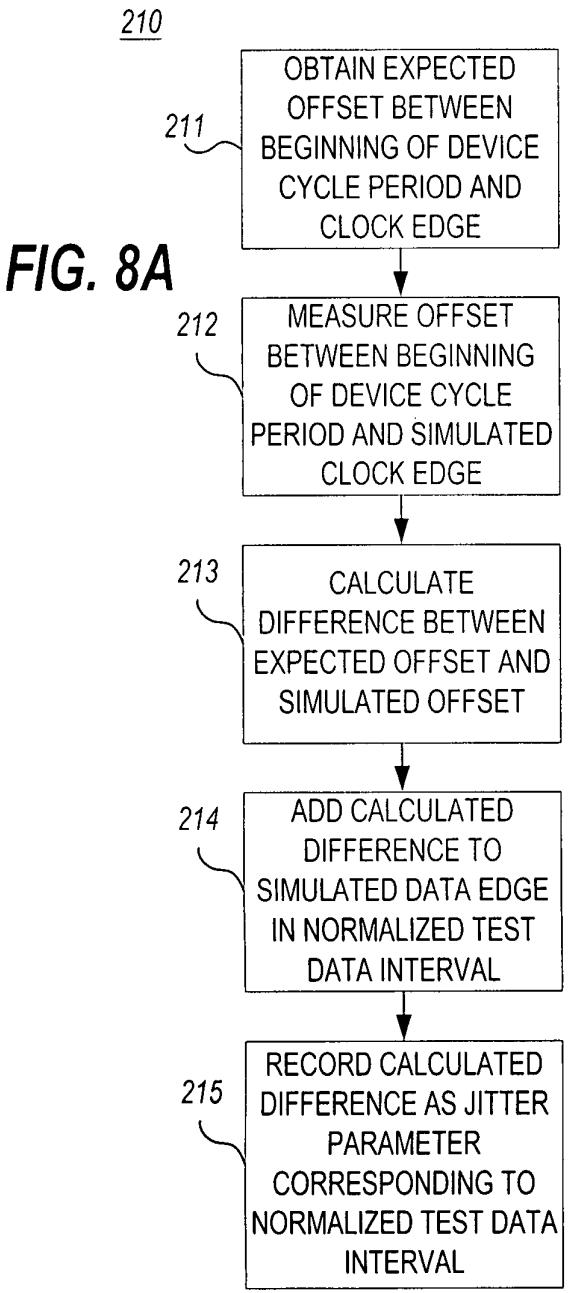
210
211
OBTAIN EXPECTED OFFSET BETWEEN BEGINNING OF DEVICE CYCLE PERIOD AND CLOCK EDGE
212
MEASURE OFFSET BETWEEN BEGINNING OF DEVICE CYCLE PERIOD AND SIMULATED CLOCK EDGE
213
CALCULATE DIFFERENCE BETWEEN EXPECTED OFFSET AND SIMULATED OFFSET
214
ADD CALCULATED DIFFERENCE TO SIMULATED DATA EDGE IN NORMALIZED TEST DATA INTERVAL
215
RECORD CALCULATED DIFFERENCE AS JITTER PARAMETER CORRESPONDING TO NORMALIZED TEST DATA INTERVAL

FIG. 8A

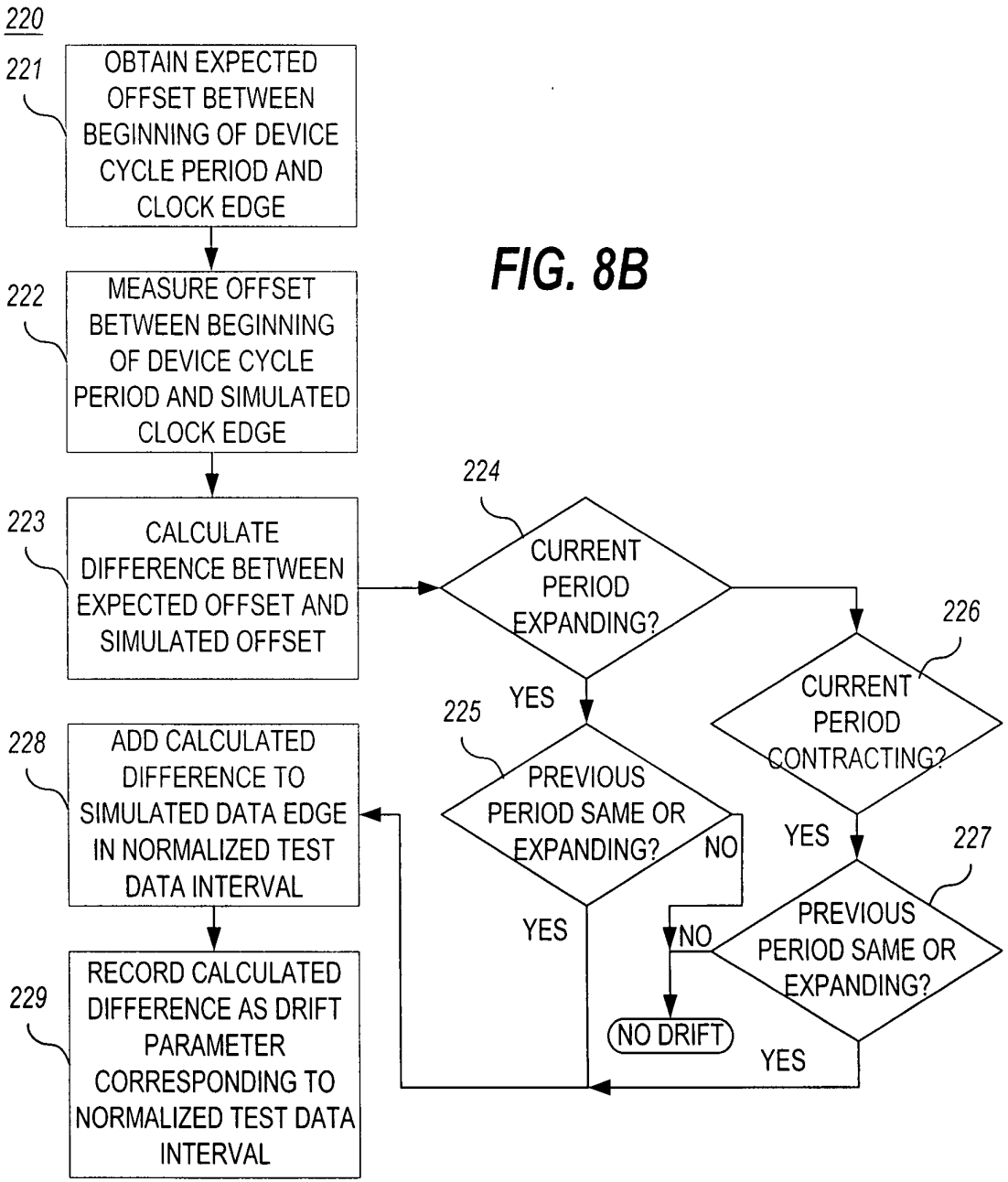
220
221
OBTAIN EXPECTED OFFSET BETWEEN BEGINNING OF DEVICE CYCLE PERIOD AND CLOCK EDGE
222
MEASURE OFFSET BETWEEN BEGINNING OF DEVICE CYCLE PERIOD AND SIMULATED CLOCK EDGE
223
CALCULATE DIFFERENCE BETWEEN EXPECTED OFFSET AND SIMULATED OFFSET
224
CURRENT PERIOD EXPANDING?
YES
225
PREVIOUS PERIOD SAME OR EXPANDING?
NO
YES
226
CURRENT PERIOD CONTRACTING?
YES
227
PREVIOUS PERIOD SAME OR EXPANDING?
NO
NO DRIFT
YES
228
ADD CALCULATED DIFFERENCE TO SIMULATED DATA EDGE IN NORMALIZED TEST DATA INTERVAL
229
RECORD CALCULATED DIFFERENCE AS DRIFT PARAMETER CORRESPONDING TO NORMALIZED TEST DATA INTERVAL

FIG. 8B

```
$ date
        2/28/2004 1:30:15 PM
$end

$version
        Jitter Example
$end

$timescale
        1ps
$end

$scope module U $end
$var wire 1 !! 
$var wire 1 !!RxD ReceiveData
$end
$var wire 1 !!RxCLK ReceiveClock
$end
$upscope $end

$enddefinitions $end

#0
$dumpvars
0!!RxCLK
1!!RxD
$end
#55
1!!RxCLK
#75
0!!RxD
#105
0!!RxCLK
#125
1!!RxD
#145
1!!RxCLK
#165
0!!RxD
#210
0!!RxCLK
#230
1!!RxD
#245
1!!RxCLK
#265
0!!RxD
```

FIG. 9A

```
$ date
        2/28/2004 1:30:15 PM
$end

$version
        Drift Example
$end

$timescale
        1ps
$end

$scope module U $end
$var wire 1 !! 
$var wire 1 !!RxD ReceiveData
$end
$var wire 1 !!RxCLK ReceiveClock
$end
$upscope $end

$enddefinitions $end

#0
$dumpvars
0!!RxCLK
1!!RxD
$end
#55
1!!RxCLK
#75
0!!RxD
#110
0!!RxCLK
#125
1!!RxD
#165
1!!RxCLK
#165
0!!RxD
#220
0!!RxCLK
#230
1!!RxD
#275
1!!RxCLK
#265
0!!RxD
```

FIG. 10A

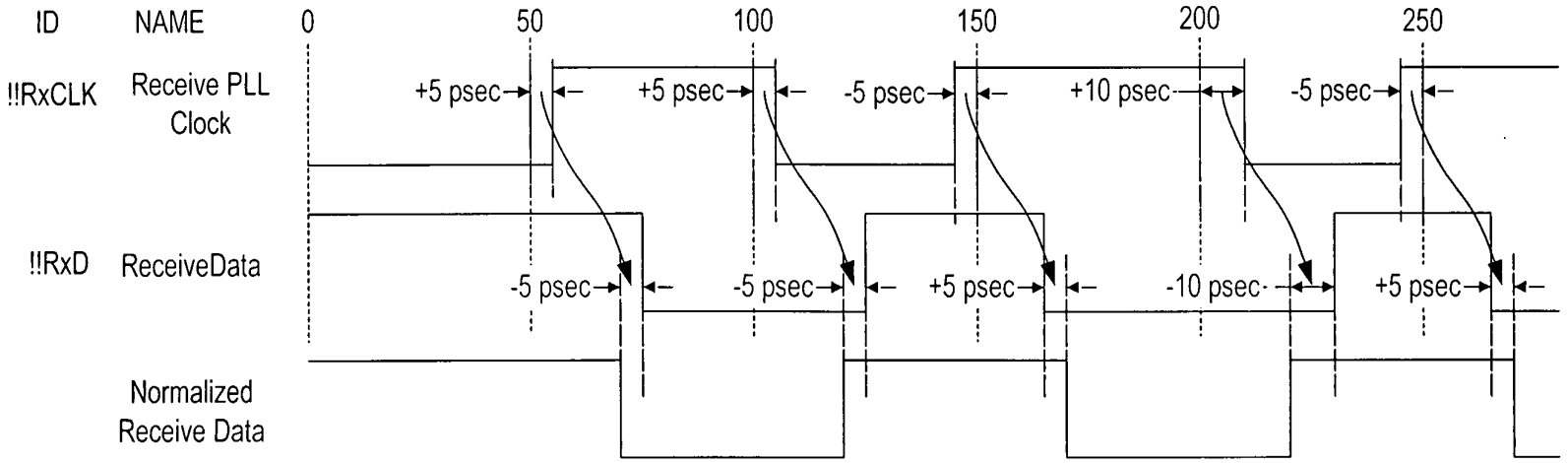

FIG. 9B

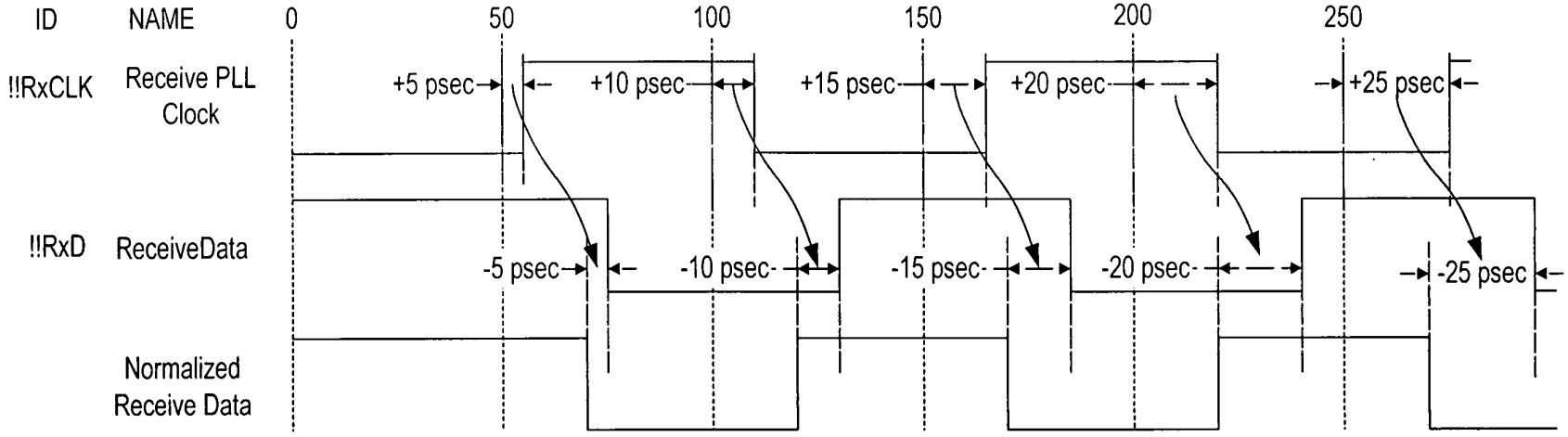

FIG. 10B

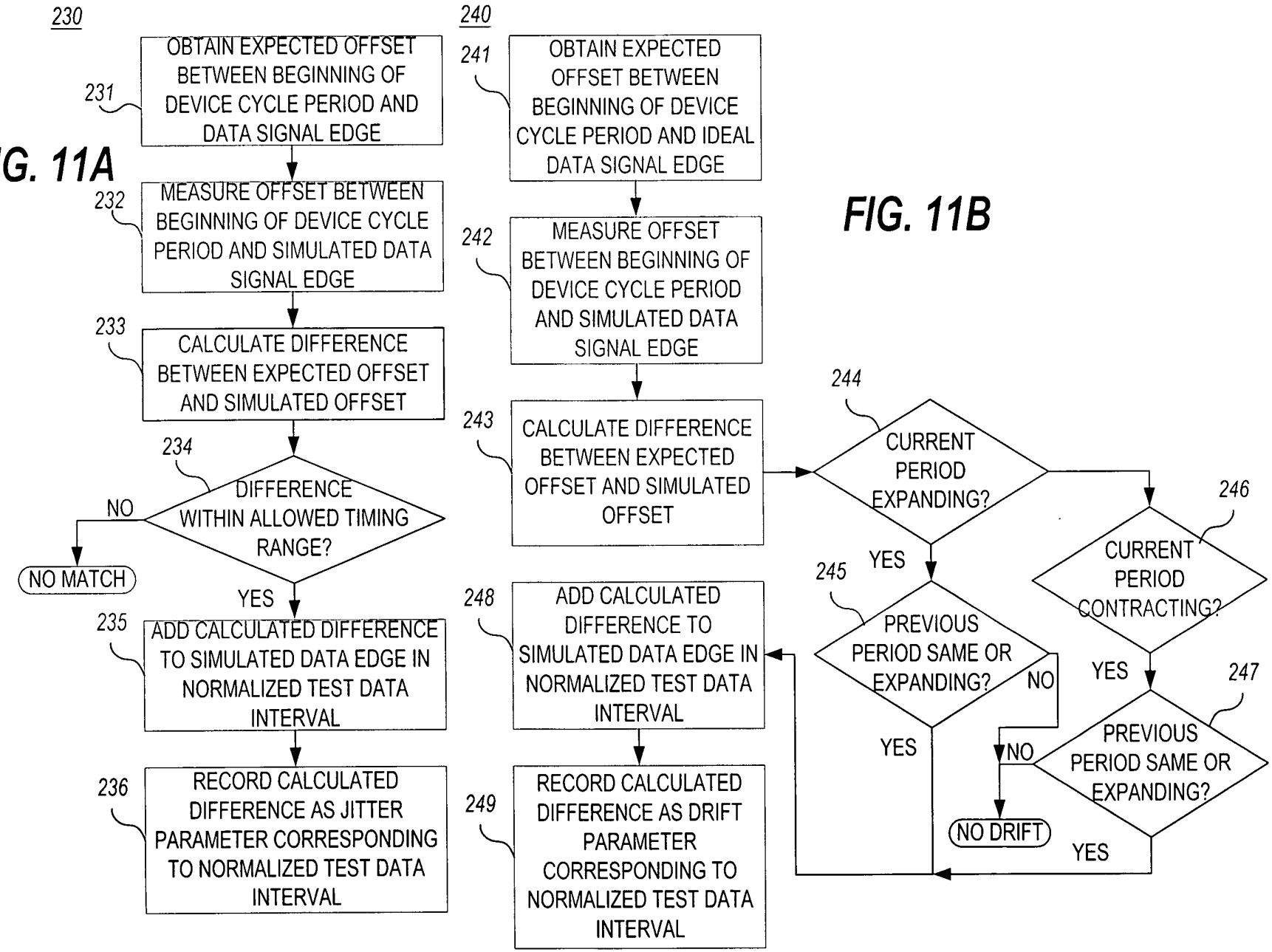

FIG. 11A

FIG. 11B